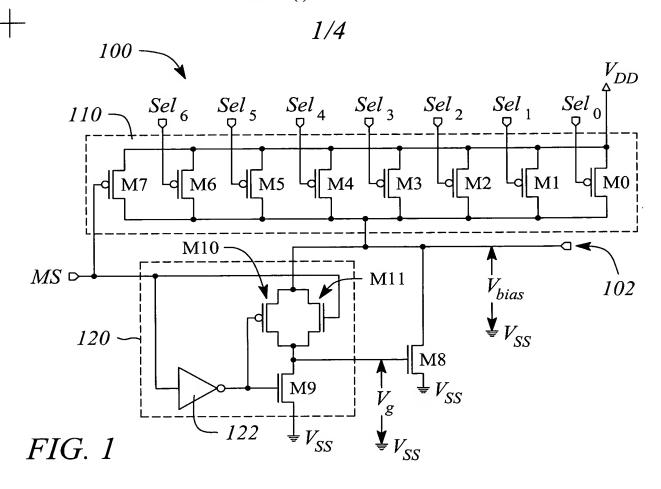Hewlett-Packard Company
Attorney Docket No. 200207084-1
Title: "Programmable Weak Write Test Mode (PWWTM)
Bias Generation Having Logic High Output Default Mode"
Inventor(s): John Wuu et al.

1/4

FIG. 1

FIG. 2
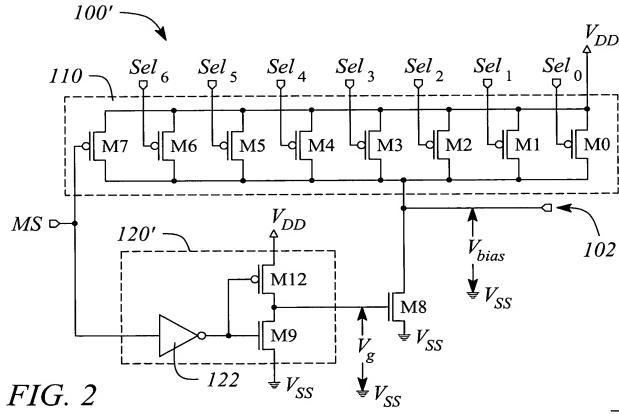
Hewlett-Packard Company
Attorney Docket No. 200207084-1
Title: "Programmable Weak Write Test Mode (PWWTM)
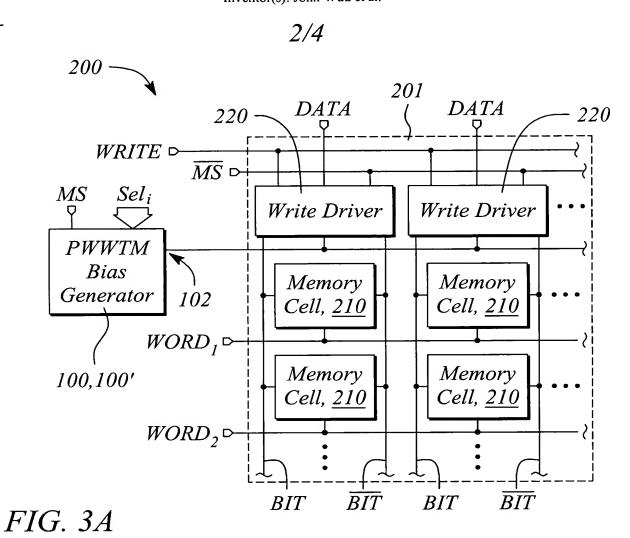Bias Generation Having Logic High Output Default Mode"
Inventor(s): John Wuu et al.

2/4

200

220 — DATA *201* DATA — *220*

WRITE

$\overline{MS}$

MS Sel_i

PWWTM
Bias
Generator *102*

100,100'

Write Driver   Write Driver   · · ·

Memory
Cell, *210*   Memory
Cell, *210*   · · ·

WORD$_1$

Memory
Cell, *210*   Memory
Cell, *210*   · · ·

WORD$_2$

BIT $\overline{BIT}$ BIT $\overline{BIT}$

FIG. 3A

V_{DD} WRITE   *220*

223

222

M21   M25   BIT

M22

$\overline{MS}$

DATA

M23   M26 $\overline{BIT}$

M24

M28   M27

V_{SS}

224

WRITE

V_{DD}

AWWTM Input

FIG. 3B

Hewlett-Packard Company
Attorney Docket No. 200207084-1
Title: "Programmable Weak Write Test Mode (PWWTM)
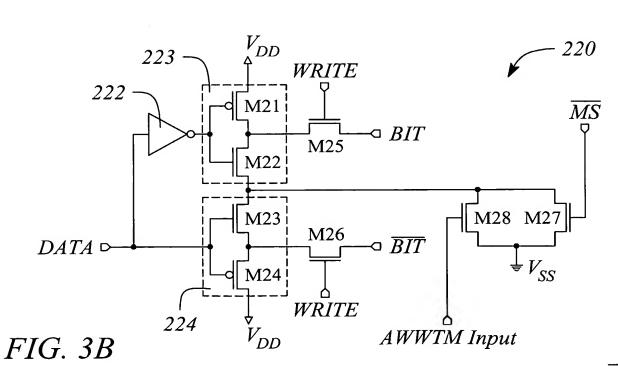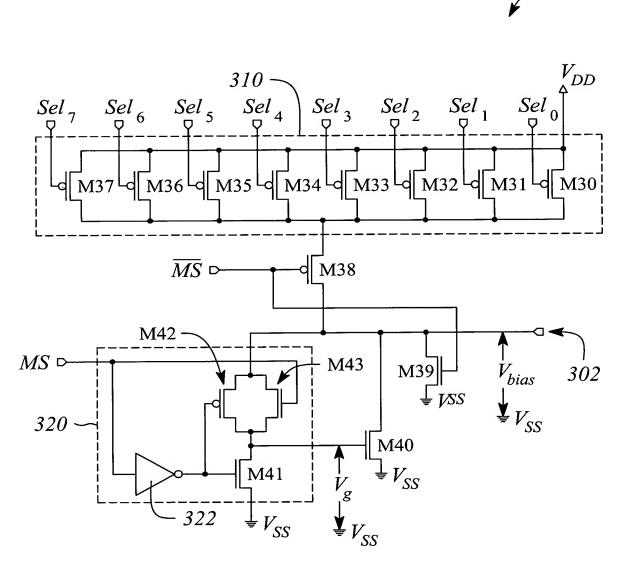Bias Generation Having Logic High Output Default Mode"
Inventor(s): John Wuu et al.

3/4

300

310

Sel_7 Sel_6 Sel_5 Sel_4 Sel_3 Sel_2 Sel_1 Sel_0 V_{DD}

M37 M36 M35 M34 M33 M32 M31 M30

$\overline{MS}$ M38

M42 M43

MS

320

M39 V_{SS}

V_{bias} *302* V_{SS}

M41 M40 V_{SS}

322 V_{SS}

V_g V_{SS}

Prior Art

FIG. 4

Hewlett-Packard Company
Attorney Docket No. 200207084-1
Title: "Programmable Weak Write Test Mode (PWWTM)
Bias Generation Having Logic High Output Default Mode"
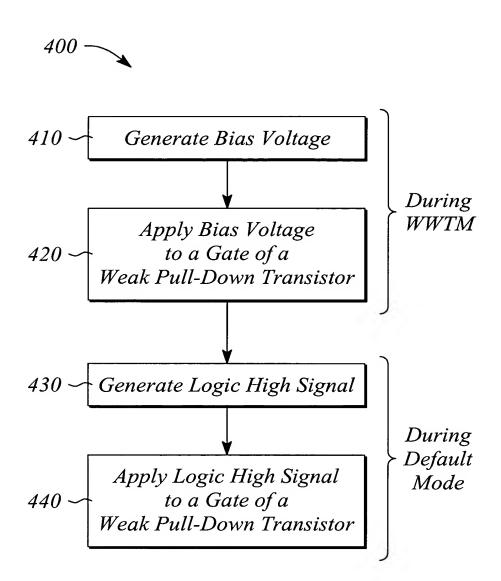Inventor(s): John Wuu et al.

4/4

400

410 — Generate Bias Voltage

420 — Apply Bias Voltage to a Gate of a Weak Pull-Down Transistor

During WWTM

430 — Generate Logic High Signal

440 — Apply Logic High Signal to a Gate of a Weak Pull-Down Transistor

During Default Mode

FIG. 5